

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Daisuke Kawagoe  
Serial No.: 10/646,478  
Filed: August 22, 2003  
Title: STACKED VIA STRUCTURE THAT INCLUDES A SKIP VIA  
Customer No. 21186

Examiner: Ishwar Patel  
Group Art Unit: 2841  
Docket: 884.937US1

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF  
Commissioner for Patents  
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Alexandria, VA 22313-1450

The applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal. The review is requested for the reason(s) stated below:

As part of making the rejection of claims 40-44 were rejected under 35 USC § 102(e) as being anticipated by Carpenter (U.S. 6,810,583), the Examiner states at page 2 of the Final Office Action that

“Carpenter, in figure 6, discloses a substrate comprising: . . . a second conductive layer (C2, as marked up on figure 6 in appendix "A"); between the second dielectric layer and the third dielectric, the second conductive layer including a first skip via (57) that extends through the first and second dielectric layers; and a third conductive layer (C3) on the third dielectric layer, the third conductive layer including a second via (26) that extends through the third dielectric layer, the second via and the first skip via being stacked on to of one another (see marked up figure 6 in appendix "A").”

Applicant respectfully traverses these assertions. Applicant respectfully refers to the Examiner's marked up drawing which shows that the layer C2 (indicated by the Examiner as the second conductive layer) does not include any vias. Applicant notes that each of the vias is shown as a separate entity from the marked C2 layer. Applicant further notes that each of vias 55, 56, 57, 58 in Carpenter are shown with separate cross-hatching from the corresponding metallizations 21, 31, 28, 29 in the metallic layer 14. Since the vias 55, 56, 57, 58 in Carpenter are not part of the metallic layer 14 (indicated as the C2 layer by the Examiner), Carpenter does not teach or suggest “the second conductive layer including a first skip via that extends through the first and second dielectric layers” as recited in claim 40.

Applicant also respectfully refers to the Examiner's marked up drawing which shows that the layer C3 (indicated by the Examiner as the third conductive layer) does not include any vias.

Applicant notes that each of the vias is shown as a separate entity from the marked C3 layer. Therefore, Carpenter does not teach or suggest "the third conductive layer including a second via that extends through the third dielectric layer" as recited in claim 40.

The Examiner states at page 13 of the Final Office Action that

"The applicant argues that layer C2 (second conductive layer) does not include any vias. Therefore, Carpenter does not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers". This is not found to be correct. Via (57) as shown in marked up figure 6 (appendix "A"), does extend through dielectric layer D1 and D2 and is connected with the conductive layer (C2)."

Applicant respectfully traverses these assertions in part because even though via 57 extends through dielectric layers D1 and D2 (reference numbers 41 and 43 in Carpenter), and is connected to metallization 28 in metallic layer 14, the via 57 is not part of the metallic layer 14 as indicated by the separate cross-hatching in Figure 6. Applicant notes that the dielectric layer 41 is connected to the metallic layer 14, but Applicant respectfully submits that just as with via 57, the dielectric layer 41 is not part of metallic layer 14. Since the vias 55, 56, 57, 58 in Carpenter are not part of the metallic layer 14, Carpenter does not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers" as recited in claim 40.

The Examiner also states at page 13 of the Final Office Action that

"Applicant further argues that layer C3 (third conductive layer in marked up figure 6 (appendix "A")) does not include any via. Therefore, carpenter does not teach or suggest "the third conductive layer including a second via that extends through the third dielectric layer". This is not found to correct. Via (26) as shown in marked up figure 6 (appendix "A"), does extend through the dielectric layer D3 and is connected with the conductive layer (C3)."

Applicant respectfully traverses these assertions in part because even though via 26 extends through dielectric layer D3 (reference numbers 13 and 15 in Carpenter), and is connected to metallization 87 in metallic layer 116, the via 26 is not part of the metallic layer 116 as indicated by the separate cross-hatching in Figure 6. Applicant notes that the dielectric layer 15 is connected to the metallic layer 116, but Applicant respectfully submits that just as with via 26, the dielectric layer 15 is not part of metallic layer 116. Since none of the vias in Carpenter are part of any metallic layer, Carpenter does not teach or suggest "the third

conductive layer including a second via that extends through the third dielectric layer" as recited in claim 40.

As part of making the rejection of claims 47-51 under 35 USC § 102(e) as being anticipated by Carpenter (U.S. 6,810,583), the Examiner states at page 4 of the Final Office Action that

"Carpenter, in figure 7, discloses a substrate comprising: . . . a second conductive layer (C3, marked up on figure 7 in appendix "B") between the second and third dielectric layers, the second conductive layer including a first skip via (VI, marked up on figure 7 in appendix "B") that extends through the first and second dielectric layers; a fourth dielectric layer (D4, marked up on figure 7 in appendix "B"), the third dielectric layer being between the second and fourth dielectric layers; a third conductive layer (C4, marked up on figure 7 in appendix "B") between the third and fourth dielectric layers; and a fourth conductive layer (C5, marked up on figure 7 in appendix "B") on the fourth dielectric layer, the fourth conductive layer including a second skip via (V2, marked up on figure 7 in appendix "B") that extends through the third and fourth dielectric layers, the second skip via and the first skip via being stacked on top of one another (see marked figure 7 in appendix "B")."

Applicant respectfully traverses these assertions. Applicant respectfully refers to the Examiner's marked up figure 7 which shows that the layer C3 (indicated by the Examiner as the second conductive layer) does not include any vias. Applicant notes that each of the vias is shown as a separate entity from the metallizations in the marked C3 layer. Applicant further notes that each of vias in Carpenter is shown with separate cross-hatching from the corresponding metallizations in the metallic layer C3. Since the vias in Carpenter are not part of the metallic layer (indicated as the C3 layer by the Examiner), Carpenter does not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers" as recited in claim 47.

Applicant also respectfully refers to the Examiner's marked up figure 7 which shows that the layer C5 (indicated by the Examiner as the fourth conductive layer) does not include any vias. Applicant notes that each of the vias is shown as a separate entity from the marked C5 layer. Applicant further notes that each of vias in Carpenter is shown with separate cross-hatching from the corresponding metallizations in the metallic layer C5. Therefore, Carpenter does not teach or suggest "the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers" as recited in claim 47.

The Examiner states at page 13 of the Final Office Action that

“Similarly regarding the independent claim 47, the applicant argues that Carpenter does not disclose or teach the second conductive layer including a first skip via that extends through the first and second dielectric layers and the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers. This is not found to be correct. Via (V1, as shown in figure 7, appendix B) extend through dielectric layers D1 and D2 and is connected to conductive layer C3. Similarly Via (V2) extend through dielectric layer D3 and D4 and connected to conductive layer C5.”

Applicant respectfully traverses these assertions in part because even though via V1 (as indicated by the Examiner in marked up Figure 7) extends through dielectric layers D1 and D2, and is connected to a metallization in metallic layer C3, the via V1 is not part of the metallic layer C3 as indicated by the separate cross-hatching in Figure 7. Applicant notes that the dielectric layer D2 is connected to the metallic layer C3, but Applicant respectfully submits that just as with via V1, the dielectric layer D2 is not part of metallic layer C3. Since the via V1 in Carpenter is not part of the metallic layer C3, Carpenter does not teach or suggest “the second conductive layer including a first skip via that extends through the first and second dielectric layers” as recited in claim 47.

Applicant also respectfully traverses these assertions in part because even though via V2 (as indicated by the Examiner in marked up Figure 7) extends through dielectric layers D3 and D4, and is connected to a metallization in metallic layer C5, the via V2 is not part of the metallic layer C5 as indicated by the separate cross-hatching in Figure 7. Applicant notes that the dielectric layer D4 is connected to the metallic layer C5, but Applicant respectfully submits that just as with via V2, the dielectric layer D4 is not part of metallic layer C5. Since the via V2 in Carpenter is not part of the metallic layer C5, Carpenter does not teach or suggest “the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers, the second skip via and the first skip via being stacked on top of one another” as recited in claim 47.

As part of making the rejection of claims 54-56 under 35 USC § 103(a) as being unpatentable over Carpenter, the Examiner states at page 6 of the Final Office Action that “Carpenter discloses all the features of the claimed invention as applied to claim 47 above, . . .”.

As discussed above, Applicant respectfully traverses this assertion and notes that the cited reference has no teaching or suggestion as to any of the conductive layers including a via.

As part of making the rejection of claims 45, 46, 52, 53, 57 and 58 were also rejected under 35 USC § 103(a) as being unpatentable over Carpenter, and further in view of Uchikawa (U.S. 6,531,661) and Asai (U.S. 6,534,723), the Examiner states at page 7 of the Final Office Action that “Carpenter discloses all the features of the claimed invention as applied to claim 40 above.”

Applicant respectfully traverses this assertion. As discussed above, Carpenter does not teach or suggest “the second conductive layer including a first skip via that extends through the first and second dielectric layers” or “the third conductive layer including a second via that extends through the third dielectric layer” as recited in claim 40.

The Examiner further states at page 9 of the Final Office Action that “Carpenter discloses all the features of the claimed invention as applied to claim 47 above . . .” Applicant respectfully traverses this assertion. As discussed above, Carpenter does not teach or suggest “the second conductive layer including a first skip via that extends through the first and second dielectric layers” or “the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers” as recited in claim 47.

### **CONCLUSION**

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at (262) 646-7009 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,  
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